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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/121,175	07/22/1998	RICHARD B. MERRILL	FOV-011	3033

7590 01/16/2003

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EXAMINER

YE, LIN

ART UNIT	PAPER NUMBER
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2612

DATE MAILED: 01/16/2003

22

Please find below and/or attached an Office communication concerning this application or proceeding.

11

Office Action Summary

Application No.

09/121,175

Applicant(s)

MERRILL ET AL.

Examiner

Lin Ye

Art Unit

2612

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 31 October 2002.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-9, 21-29, 31-36 and 48-57 is/are pending in the application.

4a) Of the above claim(s) 1-9, 21-29, 31-36 and 48-57 is/are withdrawn from consideration.

- 5) ☐ Claim(s) 10-20, 37-47, 58-59 is/are allowed.

- 6) ☒ Claim(s) 1-9, 21-29, 31-36 and 48-57 is/are rejected.

- 7) ☐ Claim(s) 10-20, 37-47, 58-59 is/are objected to.

- 8) ☐ Claim(s) 10-20, 37-47, 58-59 are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on 10-20, 37-47, 58-59 is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on 10-20, 37-47, 58-59 is: a) ☐ approved b) ☐ disapproved by the Examiner.
If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. .
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
* See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892) 4) ☐ Interview Summary (PTO-413) Paper No(s).
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948) 5) ☐ Notice of Informal Patent Application (PTO-152)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 20. 6) ☐ Other:

DETAILED ACTION

Response to Arguments

1. Applicant's arguments with respect to claims 1-9, 21-29, 31-36 and 48-54 filed on 10/31/02 have been considered but are moot in view of the new ground(s) of rejection.
2. Applicant's arguments filed 10/31/02 have been fully considered but they are not persuasive as to claims 55-57.

For claims 55-57, the applicant argues that Merrill fails to disclose a means ... for outputting a value from any of said plurality of storage nodes comprising. However, those features are not recited in the claim 55. Except the only place state this arrangement ("outputting a value from any of said plurality of storage nodes is in the preamble of amended claim 55. The preamble does not anticipate this claim. In order to give the preamble patentable weight, the preamble must be "essential to point out the invention defined by the claim." (Kropa v. Robie, 187 F.2d 150, 888 USPQ 478, 481 (CCPA 1951)).

Claim Rejections - 35 USC § 112

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claim 3 (line 2) recites the limitation "said" in "said plurality of transfer lines". There is insufficient antecedent basis for this limitation in the claim, because claim 1 only claims one transfer line.

Art Unit: 2612

5. Claims 5 and 32 (line 2) recite the limitation "said " in "said storage elements". There is insufficient antecedent basis for this limitation in the claim, because claim 1 only claims storage nodes.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

7. Claims 1-3, 5, 28-29 and 32 are rejected under 35 U.S.C. 102(e) as being anticipated by Bailey et al. U.S. Patent 56,243,134.

Referring to claim 1, the Bailey reference discloses in Figures 5 and 7, an active pixel sensor (CMOS sensor 514 in figure 7) disposed on a semiconductor substrate, comprising a photosensor (photodiode PD2, See Col 6, lines 30-31) having a first terminal and a second terminal, said first terminal coupled to a first reference potential; a reset transistor (transistor M10) having a first terminal coupled to said second terminal of said photosensor, a second terminal coupled to a reset potential, and a third terminal coupled to a reset line (See Col 6, lines 53-64); a plurality of transfer transistors (M11 or M12), each transfer transistor having a first terminal connected to said second terminal of said photosensor, a second terminal, and a third terminal connected to a transfer line; and a plurality of storage nodes (nodes D, E with

Art Unit: 2612

storage elements C2 and C3) , each storage node coupled to a separate one of said second terminal of said plurality of transfer transistors (M11 or M12) as shown in Figure 5.

Referring to claim 2, an active pixel sensor (CMOS sensor 514) further including means coupled to plurality of storage nodes (nodes D, E with storage elements C2 and C3) for outputting a value from any of said plurality of storage nodes (See. Col. 7, lines 20-24).

Referring to claim 3, an active pixel sensor (CMOS sensor 514) includes a plurality of transfer lines (lines of sample 1 and sample 2), wherein each of plurality of transfer lines is connected to a separate one of said third terminal of said plurality of transfer transistors (M11 or M12).

Referring to claim 28. An active pixel sensor (CMOS sensor 514) disposed on a semiconductor substrate, comprising: comprising a photosensor (PD2) having a first terminal and a second terminal, said first terminal coupled to a first reference potential; a reset transistor (M10) having a first terminal coupled to said second terminal of said photosensor, a second terminal coupled to a reset potential, and a third terminal coupled to a reset line; and a plurality of transfer transistors (M11 or M12), each transfer transistor having a first terminal connected to said second terminal of said photosensor, a second terminal, and a third terminal connected to a transfer line; and a plurality of storage nodes (nodes D, E with storage elements C2 and C3) , each storage node coupled to a separate one of said second terminal of said plurality of transfer transistors (M11 or M12) as shown in Figure 5.

Referring to claim 29 is considered substantively equivalent to claim 2 discussed above.

Referring to claim 32 is considered substantively equivalent to claim 5 discussed above.

Art Unit: 2612

8. Claims 55-57 are rejected under 35 U.S.C. 102(e) as being anticipated by Merrill et al. U.S. Patent 5,962,844 (Hereinafter referred to as Merrill).

Referring to claim 55, the Merrill reference discloses in Figure 8A, a method of operating an active pixel sensor having a photosensor (402), a reset transistor (404), a plurality of storage nodes (node 1 & 2) coupled to said photosensor and means coupled to said plurality of storage nodes for outputting a value (See Col 9, Table 1, a voltage value = $v_2 - v_1$ output from node 1 and a voltage value = $v_3 - v_2$ output from node 2) from any of said plurality of storage nodes comprising: turning on the reset transistor to place a reset potential on said photosensor; transferring charge from said photosensor (400) to a first of the plurality of storage nodes (node 1) for a first duration; and transferring charge from said photosensor to a second of the plurality of storage nodes for a second duration (See Col. 9, lines 5-13).

Referring to claim 56, a method of operating an active pixel (400) includes wherein said first duration commences coincident with said second duration (See Col. 9, lines 20-29, the new integrated output starts end of the current integration interval).

Referring to claim 57, a method of operating an active pixel (400) includes wherein said second duration commences after said first duration has ended (See Col. 9, lines 30-35).

9. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Art Unit: 2612

10. Claims 4,6-9, 21-27, 31, 33-36 and 48-54 are rejected under 35 U.S.C. 103(a) as being unpatentable over Beiley et al. U.S. Patent 56,243,134 in view of Merrill et al. U.S. Patent 5,962,844.

Referring claims 4,6, 21, 31, 33 and 48, the Beiley reference disclose all subject matter as discussed in respected claims 1-2 and 28-29, except the reference does not explicitly show any of said plurality of storage nodes by a separate one of a plurality of readout transistors and row select transistors having a first terminal connected to said separate one of said plurality of storage nodes. It only shows one readout transistor (M13) and row select transistor (M14) connected to separate one of plurality of storage nodes (D and E), and output values from the nodes (E and D) is separate and followed each other (See Figure 6, in time T5-T6, the output value R is related node E. In time T7-T8, the sampled value S is related node D).

The Merrill reference discloses in Figures 8A, 4 and 3, an active pixel sensor (400) includes each separate one of said plurality of storage nodes is coupled to said means for outputting a value from any of said plurality of storage nodes by a separate one of a plurality of readout transistors (414 & 416, Col. 8, line 66) having a first terminal connected to said separate one of said plurality of storage nodes, a second terminal coupled to a second potential, and a third terminal connected to said means for outputting a value from any of said plurality of storage nodes ; a plurality of column output lines (202 & 204); a row select line (128); and a plurality of row select transistors (n3 and n5), each of said row select transistors having a first terminal coupled to one of said plurality of storage nodes, a second terminal coupled to one of said plurality of column output lines, and a third terminal coupled

Art Unit: 2612

to said row select line (See Col. 8, lines 66-67). The Merrill reference is an evidence that one of ordinary skill in the art at the time to see more advantages for an active pixel image cell has one of plurality of readout transistors and row select transistors to connect with separate one of said plurality of storage nodes, because it can simultaneously generate as pixel output the signals required for determining the difference between the pixel output and increase the speed with which images can be acquired. For that reason, it would have been obvious to see the any of said plurality of storage nodes by a separate one of a plurality of readout transistors and row select transistors having a first terminal connected to said separate one of said plurality of storage nodes disclosed by Bailey.

Referring to claim 7, the Merrill reference discloses an active pixel sensor (400) including plurality of transfer lines (x & \bar{x}), wherein each separate one of plurality of storage nodes is coupled to said second terminal of said photosensor (402) by a separate one of a plurality of transfer transistors (406 & 408) having a first terminal connected to said second terminal of said photosensor (402), a second terminal connected to said separate one of said plurality of storage nodes, and a third terminal connected to a separate one of said plurality of transfer lines (x & \bar{x}).

Referring to claim 8, the Merrill reference discloses an active pixel sensor (400) has wherein each separate one of said plurality of storage nodes (node 1 & 2 with storage elements 410 & 412) is coupled to said first terminal of a separate one of said plurality of row select transistors (418) by a separate one of a plurality of readout transistors having a first terminal connected to said separate one of said plurality of storage nodes, a second

Art Unit: 2612

terminal coupled to a second potential, and a third terminal coupled to said first terminal of said separate one of said plurality of row select transistors.

Referring to claim 9, the Merrill reference discloses an active pixel sensor (400) includes a plurality of storage elements (node 1 & 2 with storage elements 410 & 412), each separate one of said storage elements having a first terminal coupled to a separate one of said storage nodes, and a second terminal coupled to a second reference potential.

Referring to claim 22, the Merrill reference discloses an active pixel sensor (100 or 400), further including a plurality of transfer lines, wherein each separate one of said plurality of storage nodes is coupled to said second terminal of said photosensor by a separate one of a plurality of transfer transistors having a first terminal connected to said second terminal of said photosensor, a second terminal connected to said separate one of said plurality of storage nodes, and a third terminal connected to a separate one of said plurality of transfer lines.

Referring to claim 23, the Merrill reference discloses an active pixel sensor (100 or 400) wherein each separate one of said plurality of storage nodes is coupled to said first terminal of one of said plurality of row select transistors by a separate one of a plurality of readout transistors having a first terminal connected to said one of said plurality of storage nodes, a second terminal coupled to a second potential, and a third terminal coupled to said first terminal of said one of said plurality of row select transistors as shown in figure 4.

Referring to claim 24, the Merrill reference discloses an active pixel sensor (100 or 400), further including a plurality of storage elements, each separate one of said storage elements having a first terminal coupled to a separate one of said storage nodes, and a second terminal coupled to a second reference potential.

Referring to claim 25, the Merrill reference discloses an active pixel sensor (100 or 400), wherein said means for outputting a value includes: a row select line (128); a column bias line; first and second column output lines; a row select transistor having a first terminal coupled to said row select line, second terminal coupled to said column bias line, and a third terminal; and wherein said plurality of storage nodes includes a first node and second storage node, said first storage node is coupled to said means for outputting a value by a first readout transistors having a first terminal coupled to said first storage node, a second terminal coupled to said first column output line, and a third terminal connected to said third terminal of said row select transistor (418 or n3 and n5), and said second storage node is coupled to said means for outputting a value by a second readout transistor having a first terminal coupled to said second storage node, a second terminal coupled to said second column output line, and a third terminal connected to said third terminal of said row select transistor (418 or n3 and n5).

Referring to claim 26, the Merrill reference discloses an active pixel sensor (100 or 400), further including a plurality of transfer lines (x & xbar), wherein each separate one of said plurality of storage nodes is coupled to said second terminal of said photosensor by a separate one of a plurality of transfer transistors having a first terminal connected to said second terminal of said photosensor, a second terminal connected to said separate one of said plurality of storage nodes, and a third terminal connected to a separate one of said plurality of transfer lines.

Referring to claim 27, the Merrill reference discloses an active pixel sensor (400), further including a plurality of storage elements (410 & 412), each separate one of said storage

Art Unit: 2612

elements having a first terminal coupled to a separate one of said storage nodes, and a second terminal coupled to a second reference potential.

Referring to claim 34 is considered substantively equivalent to claim 7 discussed above.

Referring to claim 35 is considered substantively equivalent to claim 8 discussed above.

Referring to claim 36 is considered substantively equivalent to claim 9 discussed above.

Referring to claim 49 is considered substantively equivalent to claim 22 discussed above.

Referring to claim 50 is considered substantively equivalent to claim 23 discussed above.

Referring to claim 51 is considered substantively equivalent to claim 24 discussed above.

Referring to claim 52 is considered substantively equivalent to claim 25 discussed above.

Referring to claim 53 is considered substantively equivalent to claim 26 discussed above.

Referring to claim 54 is considered substantively equivalent to claim 27 discussed above.

Conclusion

11. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a).

Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event,

Art Unit: 2612

however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to **Lin Ye** whose telephone number is **(703) 305-3250**. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wendy R Garber can be reached on (703) 305-4929.

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks

Washington, DC. 20231

Or faxed to:

(703) 872-9314

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal drive,
Arlington, VA., Sixth Floor (Receptionist).

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Technology Center 2600 Customer Service Office whose telephone number is (703) 306-0377.

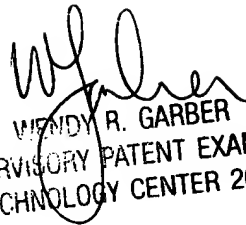
Application/Control Number: 09/121,175

Page 12

Art Unit: 2612

Lin Ye

January 13, 2003


WENDY R. GARBER
SUPERVISORY PATENT EXAMINER
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